DOCKET NO. 00-BN-059 (STMI01-00059) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

CLAIM REJECTIONS -- 35 U.S.C. §103(a)

Claims 1-22 were rejected as being unpatentable over U.S. Patent No. 5,819,058 to Miller et al. ("Miller") in view of U.S. Patent No. 6,167,503 to Jouppi ("Jouppi"). The final rejection is legally and factually deficient for two reasons:

1. The rejections of the independent claims rely on factually incorrect allegations of the teachings of the prior art;
2. The rejections of the independent claims are legally deficient in that they include no showing at all that specific claim limitations are taught or suggested in the prior art reference.

Claim 1 requires an "instruction issue unit" that issues "complete instruction bundles" toward multiple execution clusters, where at least one complete instruction bundle is "issued having an out-of-order alignment." Claim 1 also requires "alignment and dispersal circuitry" capable of "reordering each of the at least one complete instruction bundle having the out-of-order alignment" so as to "align the syllables in the complete instruction bundle with correct ones of the lanes."

In her Advisory Action, Examiner Li for the first time indicates that she believes that Miller's "decompressor" 178 functions as the claimed "instruction issue unit". Examiner Li's belief is in error.

Claim 1 requires that the instruction issue unit be capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward the execution clusters, where at least one complete instruction bundle is issued having an out-of-order alignment.

Examiner Li indicates that this is satisfied by Miller's decompressor 178, which receives compressed instructions, uncompresses them, and puts the resulting very long instruction word 292 into a very long instruction register 180. Various bits of the register 180, forming specific instructions, are then read by an execution control unit (ECU) 26, multiplier unit (MUL) 30, an arithmetic logic unit (ALU) 32, register control unit (RCU) 34, and memory unit (MEM) 36, which Miller considers each to be a "processing unit".

Even assuming (without conceding) that Miller's very long instruction word 292 corresponds to the claimed "complete instruction bundle", nothing in Miller teaches or suggests that at least one complete instruction bundle is issued having an out-of-order alignment. Examiner Li makes reference to Miller's discussion of "default instructions" in col. 9-10, where Miller describes that default instructions can be inserted where the end of a compressed packet is detected. Here, nothing indicates that any of the actual instruction are out of order – using default instructions for a processor that has no compressed instruction does not imply that the actual instructions for other processors are therefore out-of-order, and Miller makes no teaching or suggestion that this is the case.

Claim 1 also requires alignment and dispersal circuitry capable of receiving said complete instruction bundles from the instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles. The Examiner alleges that Miller's multiplexers 224, 226, 228, 230, 232 satisfy this element. However, claim 1 also requires that the alignment and dispersal circuitry be also capable of reordering the complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with

correct ones of the lanes. Nothing in Miller teaches or suggests that multiplexers 224, 226, 228, 230, 232 are capable of re-ordering the bits or syllables they receive when producing the very long instruction word 292, nor that the very long instruction register 180 can do so. Note that Examiner Li still has made no attempt at all to specifically identify where this feature is taught by Miller, and certainly has not shown where this function is taught to be performed by multiplexers 224, 226, 228, 230, 232. By failing to show where this feature of claim 1, and similar features of independent claims 10 and 19, are taught or suggested by the art of record, Examiner Li has failed to make even a *prima facie* obviousness rejection, a clear legal deficiency of the final rejection.

Further, claim 1 requires that the complete instruction bundles be issued toward a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, and wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles.

Examiner Li concedes that Miller teaches nothing like the claimed execution clusters, and refers to Jouppi. Jouppi discusses parallel execution clusters in a superscalar computer system. Evidently, Examiner Liu believes that one of skill in the art would be motivated to insert a superscalar computer system execution unit in place of each of the execution control unit, multiplier unit, an arithmetic logic unit, register control unit, and memory unit of Miller's processor, and that to do so would be more efficient and would not increase circuit complexity. The Examiner's

conclusion is believed to be factually and logically erroneous, and the combination of references therefore both unmotivated and potentially inoperable.

These are but a few of the numerous distinctions of the current claims over the cited art. Many other distinctions are present, but these suffice to show that the current claims should all be allowed over all art of record.

CONCLUSION

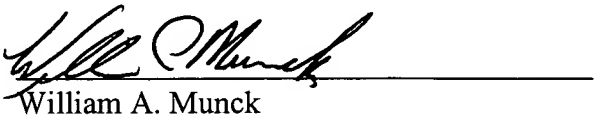
As a result of the foregoing, the Applicant asserts that the claims in the Application are in condition for allowance over all art of record, and respectfully requests this case be returned to the Examiner for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Jan 9, 2006



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